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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,062	03/31/2004	Chu Wan Hong	4459-144	5268

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,062	HONG, CHU WAN	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-10, 12, 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA) in view of Chen et al. (U.S. Patent No. 6,686,667 B2).

In re claims 1, 12 and 18-20, APA (Fig. 1) discloses a semiconductor package structure comprising:

a SAW chip (13) having a first surface, a second surface opposite to the first surface, an interdigital transducer IDT (13b) disposed on the first surface, and a plurality of first bonding pads (13c) disposed around the IDT on the first surface,

a mutli-layer ceramic substrate (14, 16c, 16b, 16a) having a cave (12) formed thereon and a plurality of second bonding pads (24) disposed around the cave and electrically connected to the first bonding pads, wherein the cave and the plurality of second bonding pads are corresponding to the IDT and the plurality of first bonding pads, respectively, and

an adhesive layer formed between the surface of the SAW chip and the multilayer ceramic substrate for tightly bonding the SAW chip and the multi-layer ceramic substrate together, wherein the first surface of the SAW chip, the adhesive layer and the cave of the multi-

layer ceramic substrate together define a cavity such that the IDT of the SAW chip is exposed within the cavity.

APA does not expressly disclose the adhesive layer formed around the cave to define a cavity such that the chip is exposed from the adhesive layer. Chen (esp. Fig. 1) discloses a adhesive castellation (160) that surrounds a chip area. It would have been obvious to one or ordinary skill in the art at the time of the invention to use adhesive castellations as disclosed by Chen in place of one of the ceramic layers of APA for the purpose, for example, of making the adhesion stronger between the substrate and the top layer (Chen; column 4, lines 43-55).

In re claim 3, APA in view of Chen discloses the device of claim 1, wherein the chip is a semiconductor chip.

In re claim 4-6, APA in view of Chen discloses the device of claim 1. The different types of chips claimed simply described the method for using this package device, and amount to mere intended use limitations. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claims 7 and 14, APA in view of Chen discloses the devices of claims 1 and 12 respectively, wherein the material of the substrate is a polymeric material (Chen discloses a substrate of organic resin, which is a polymer. Also, Huang (U.S. Patent No. 6,720,649 B2) is included as a teaching reference, to show the well known use of polymer and ceramic substrates (column 4, lnes 30-36).

In re claims 8 and 15, APA in view of Chen discloses the devices of claims 1 and 12 respectively, but does not expressly disclose gold wires contacting the bond pads. However,

gold a well known connecting layers in the semiconductor art and it would have been obvious for one of ordinary skill at the time of the invention to use a gold connecting layer between the bond pads because gold is known to have a good conductivity and also to be a good adhesive layer.

In re claims 9, 10, 16 and 17, APA in view of Chen discloses the devices of claims 1 and 12 respectively, wherein the castellation layer (160) of Chen fulfills the claimed language by being formed on the upper portion of the chip and extending downwards to protect that upper surface from moisture.

In re claim 11, APA in view of Chen discloses the device of claim 1, wherein the multi-layer ceramic substrate has a plurality of via conductors

3. Claims 2, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA/Chen as applied to claim 1 above, and further in view of Kurogi (U.S. Patent No. 5,578,874).

In re claims 2, 11 and 13, APA in view of Chen discloses the device of claims 1 and 12 respectively, but does not expressly disclose vias passing through the ceramic substrate to an external circuit. Kurogi (esp. Fig. 4) discloses a number of via conductors (34, 36) passing through a ceramic substrate (12). It would have been obvious for one skilled in the art at the time of the invention to use via conductors as disclosed by Kurogi for the device of APA/Chen for the purpose, for example, of permitting extemal connection of the internal circuit (Kurogi; column 2, lines 59-66) to the external bonding pads (26) of APA.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815